

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF:

GROUP: 2814

Motoo ASAI, et al.

SERIAL NO: 10/509,899

EXAMINER: JAHAN, BILKIS

FILED: June 29, 2005

FOR: SUBSTRATE FOR MOUNTING IC CHIP, MANUFACTURING METHOD OF
SUBSTRATE FOR MOUNTING IC CHIP, DEVICE FOR OPTICAL
COMMUNICATION, AND MANUFACTURING METHOD OF DEVICE FOR
OPTICAL COMMUNICATION

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants request review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a Notice of Appeal.

The review is requested for the reason(s) stated on the attached sheet(s). No more than five (5) pages are provided.

I am the attorney or agent of record.

Respectfully Submitted,

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PRE-APPEAL BRIEF CONFERENCE ARGUMENTS

I. Request for Discussion of Amendments that May Result in Allowance

The remarks below provide explanations and discussions on the distinctions between the claimed invention and the cited references. Applicant respectfully requests the Examiner to contact and discuss with the undersigned, should any amendments to the pending claims are deemed necessary to clarify the distinctions discussed below and place this application in condition for allowance.

II. Description of the Invention

Claims 1-71 are presently pending in this application, Claim 1 being independent and Claims 2-11 being directly or indirectly dependent from Claim 1, and Claims 12-71 having been withdrawn from further consideration by the Examiner.

Claim 1 is directed to a substrate for mounting an IC chip and recites: "an insulating substrate having a first surface and a second surface on an opposite side of the first surface; a first built-up structure formed on the first surface of the insulating substrate and comprising a conductor circuit and an interlaminar insulating layer; a second built-up structure formed on the second surface of the insulating substrate and comprising a conductor circuit and an interlaminar insulating layer; a solder resist layer formed as an outermost layer over the first built-up structure; an optical element mounted over the solder resist layer; and an optical path for transmitting optical signal to or from the optical element and penetrating through the insulating substrate, first built-up structure, second built-up structure and solder resist layer."

By providing such an optical path, the optical element can be positioned over the outer surface of the first built-up structure, and thus it can be mounted with improved accuracy in alignment and/or readily replaced if found to be defective or inoperable.

III. The Claimed Invention Is Not Obvious over the Cited References

In the outstanding Office Action, Claims 1, 2, 6-8, 10 and 11 were rejected under 35 U.S.C. §103(a) as being unpatentable over Bhatt et al. (U.S. Patent 5,822,856) in view of Kanber (U.S. Patent 5,312,765); Claims 3 and 9 were rejected under 35 U.S.C. §103(a) as being unpatentable over Bhatt et al., Kanber in view of Lee et al. (U.S. Patent 5,452,283); Claim 4 was rejected under 35 U.S.C. §103(a) as being unpatentable over Bhatt et al. , Kanber in view of Stone (U.S. Patent 5,530,288); and Claim 5 was rejected under 35 U.S.C. §103(a) as being unpatentable over Bhatt et al., Kanber in view of Lee et al. and Stone.

The outstanding Office Action states that the structure recited in Claim 1 is unpatentable over Bhatt et al. and Kanber because “[i]t would have been obvious ... to replace Bhatt’s structure with Kanber’s structure as suggested above to improve the heat dissipation efficiency and make strong substrate (col. 2, lines 38-41)” In reaching this conclusion, the Office Action states that “Bhatt does not explicitly disclose the element is an **optical** element; the path is an **optical** path for transmitting optical signal to or from the **optical** element” and that “Kanber discloses the element is an optical element 76, 84 (Fig. 12, col. 6, lines 21-22, col. 3, lines 49-50); the path is an optical path 92 (Fig. 12, col. 6, lines 38-41) for transmitting optical signal 94 to or from the optical element 76, 84.”

It is respectfully submitted that “[i]f the proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification.”¹ MPEP also states that “[i]f the proposed modification or combination of the prior art would change the principle of

¹ *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984).

operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious.”²

The ensuing Advisory Action states that “the references Bhatt and Kanber is properly combined since Kanber teaches in Fig. 12, that the substrate 10 has light penetrating path 92 and light 94 going through the path 92 in order to meet with the device 76” and that “the structure of Bhatt in view of Kanber does not change the principle of operation of the primary reference or render the reference inoperable for its intended purposes.”

However, as stated in the previous response, Bhatt et al. is clear in its summary of invention that the plated through holes are filled with an organic based conductive material possibly together with thermoconductive dielectric particles for better thermal performance or with electroconductive particles to provide conductive holes.³ On the contrary, Kanber is directed to the fabrication of a vertically stacked microelectronic device layer structure on a GaAs substrate⁴ and states that “optoelectronic devices are formed on a first surface of substrate using ion implantation.”⁵ According to Kanber, “[h]ollow vias 92 may be formed through the substrate 10 to enable an optical pattern to be incident on the devices 16”⁶ In other words, the nature of the Bhatt et al. device takes on to improve thermal performance or conductivity, and to achieve those ends, Bhatt et al. describes filling a hollow portion of a plated through hole with an organic based conductive material, leading away from “hollow vias” described in Kanber. Furthermore, Kanber simply aims to provide the formation of a *monolithic microelectronic device using selective ion implantation* and describes an optoelectronic device integrally formed in a semiconductor substrate using a portion of the semiconductor substrate and a hollow via formed through the semiconductor substrate for the

² *In re Ratti*, 270 F.2d 810, 123 USPQ 349 (CCPA 1959).

³ See, for example, Bhatt et al., column 2, lines 28-43.

⁴ See, for example, Kanber, column 1, lines 10-15.

⁵ Kanber, column 2, lines 7-8.

⁶ *Id.*, column 6, lines 38-40.

optoelectronic device layer.⁷ Thus, assuming *arguendo* that the element 614 in the Bhatt et al. structure is substituted with the optoelectronic device of Kanber, the plated through hole in the Bhatt et al. structure would not be able to facilitate optical transmission to or from the optoelectronic device. On the other hand, it is believed that the substitution of the plated through hole in the Bhatt et al. structure with the hollow vias 92 as described in Kanber would require to ignore the filling of the plated through holes for the intended purposes of improving thermal performance or providing conductive holes. As such, it is believed that the combination of the structures in Bhatt et al. and Kanber as proposed in the Office Action would involve change in the principle of operation described in both Bhatt et al. and Kanber and also render the Bhatt et al. and Kanber structures unsatisfactory for their disclosed intended purposes. Furthermore, given those differences discussed above, it is believed that the combination proposed in the Office Action is a product of hindsight guided by Applicants' disclosure and lacks a proper motivation.

Based on the foregoing discussions, it is respectfully submitted that the structure recited in amended Claim 1 is distinguishable from Bhatt et al. and Kanber, and Applicants respectfully request that the outstanding obviousness rejection based on Bhatt et al. and Kanber be withdrawn.

In addition, because neither Lee et al. nor Stone is believed to teach or suggest "an optical path for transmitting optical signal to or from the optical element and penetrating through the insulating substrate, first built-up structure, second built-up structure and solder resist layer" as recited in Claim 1, the teachings of Bhatt et al., Kanber, Lee et al. and Stone even in combination are not believed to render the structure recited in Claim 1 obvious.

For the foregoing reasons, Claim 1 is believed to be allowable. Furthermore, since Claims 2-11 depend directly or indirectly from Claim 1, substantially the same arguments set

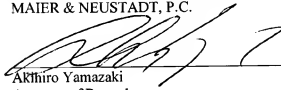
⁷ See, for example, Kanber, column 1, line 60, to column 2, line 8.

forth above also apply to these dependent claims. Hence, Claims 2-11 are believed to be allowable as well.

In view of the discussions presented above, Applicants respectfully submit that the present application is in condition for allowance, and an early action favorable to that effect is earnestly solicited.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.

A handwritten signature in black ink, appearing to read 'Arthuro Yamazaki', is written over a horizontal line.

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